

# INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)  
M4065 0197

Application Number  
Not Yet Assigned

Applicant(s)  
Wendell P. Noble, Jr., et al.

Filing Date  
Concurrently Herewith

Group Art Unit  
N/A

## U.S. PATENT DOCUMENTS

EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILED IN IF AFTER PRIORITY
KR		5,173,754	12/1992	M. Manning			
		5,214,295	05/1993	M. Manning			
		5,286,663	02/1994	M. Manning			
		5,486,717	01/1996	Kokubo et al.			
		5,497,011	03/1996	T. Terashima			
		5,535,156	07/1996	Levy et al.			
		5,581,104	12/1996	Lowrey et al.			
		5,594,683	01/1997	Chen et al.			
		5,624,863	04/1997	Helm et al.			
		5,650,350	07/1997	Dennison et al.			
KR		5,705,843	01/1998	M. C. Roberts			

## FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
							YES	NO

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

KR		R. C. Fang, LATCHUP MODEL FOR THE PARASITIC P-N-P-N PATH IN BULK CMOS, IEEE Transactions on Electron Devices, Vol. Ed. 31, No. 1, January 1984,
KR		R. R. Troutman et al, TRANSIENT ANALYSIS OF LATCHUP IN BULK CMOS, IEEE Transactions on Electron Devices, Vol. Ed. 30, No. 2, February 1993

EXAMINER  
Not Yet Assigned

DATE CONSIDERED

2/26/03

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

(Use several sheets if necessary)

~~M4065-019/P019~~  
Applicant(s)

~~Not Yet Assigned~~ 09/15/01

Wendell P. Noble, Jr., et al.

**Filing Date**

**Filing Date**  
**Concurrently Herewith**

### Group Art Unit

**N/A**

[illegible]

REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						YES	NO

KR	D. L. Hetherington ET AL, AN INTEGRATED GaAs N-P-N-P THYRISTOR/JFET MEMORY CELL EXHIBITING NONDESTRUCTIVE READ, IEEE Electron Device Letters, Vol. 13, No. 9, September 1992
KR	S. V. Vandeboek et al, HIGH-GAIN LATERAL BIPOLAR ACTION IN A MOSFET STRUCTURE, IEEE Transactions on Electron Devices, Vol. 38, No. 11, November 1991

**Not Yet Assigned**

2/26/05

**Form PTO-A820**  
**(also form PTO-1449)**

Copyright 1894-96 Legatsoff

P09A/REV02

Patent and Trademark Office • U.S. DEPARTMENT OF COMMERCE

SHEET 2 OF 3

<b>INFORMATION DISCLOSURE CITATION IN AN APPLICATION</b>				Docket Number		Application Number	
				M4065.019/P019		Not Yet Assigned	
				Applicant(s)		09/750/111	
				Wendell P. Noble, Jr., et al.			
				Filing Date		Group Art Unit	
				Concurrently Herewith		Not Assigned	
U.S. PATENT DOCUMENTS							
*EXAMINER INITIAL	REF	DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
No Citations to United States Patent Documents							
FOREIGN PATENT DOCUMENTS							
	REF	DOCUMENT	DATE	NAME	CLASS	SUBCLASS	Translations YES NO
No Citations to Foreign Patent Documents							
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)							
RR		Dermot MacSweeney et al., MODELING OF LATERAL BIPOLAR DEVICES IN A CMOS,					
		IEEE BCTM 1.4, 4 pages					
		J.J. Ebers, FOUR-TERMINAL P-N-P-N TRANSISTORS, Proceedings of IRE, Nov. 1952, p.1361-4					
		I.T. HO et al, SINGLE THYRISTOR STATIC MEMORY AND ITS FABRICATION, Vol. 23, No.3, 1980					
		B.L. Gregory et al, LATCHUP IN CMOS INTEGRATED CIRCUITS, Sandia Laboratories, p.12-18					
		S. M. Sze, PHYSICS OF SEMICONDUCTOR DEVICES, Second Edition, A Wiley Interscience Pub.					
		S.D. Malaviya, SINGLE-DEVICE DC STABLE MEMORY CELL, IBM Technical Disclosure Bulletin,					
RR		Vol. 20, No. 9, pp 3492-94, November 1978.					

EXAMINER	DATE CONSIDERED
Not Yet Assigned <i>[Signature]</i>	2/26/03
EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	